19-3858; Rev 3; 10/07

EVALUATION KIT AVAILABLE

High-Current VCOM Drive Buffers for TFT LCDs

General Description

The MAX9550/MAX9551/MAX9552 provide a VCOM source for TFT LCDs. The MAX9550/MAX9551/MAX9552 source and sink a large current to quickly restore the VCOM voltage, making it ideal for TFT LCDs. The output settles to within 0.1% in less than 2µs. In addition, the MAX9550/MAX9551/MAX9552 directly drive the capacitive load in the VCOM layer of the TFT LCDs without the need for a series resistor.

The MAX9550/MAX9551/MAX9552 feature single, dual, and quad channel VCOM amplifiers, respectively. The MAX9550/MAX9551/MAX9552 can drive up to 800mA of peak current per channel and operate up to 20V. The devices feature soft-start to reduce inrush current, output short-circuit protection, and thermal shutdown.

The MAX9550 is available in a space-saving 5-pin thin SOT23 package, and an 8-pin µMAX® package with an exposed paddle. The MAX9551 is available in an 8-pin µMAX package with an exposed paddle. The MAX9552 is available in a 14-pin TSSOP package. All devices are specified over the -40°C to +85°C temperature range.

Applications

TFT-LCD Panels

Instrument Control Voltage Sources

Pin Configuration appears at end of data sheet.

Features

- **Operates Up To 20V**
- **800mA Peak Output Current**
- **Settles to Within 0.1% of V_{OUT} in Less than 2µs**
- **Excellent Load Regulation**
- **Thermal-Shutdown Protection**
- **Short-Circuit Protection to Both Rails**
- **Soft-Start to Reduce Inrush Current**

Ordering Information

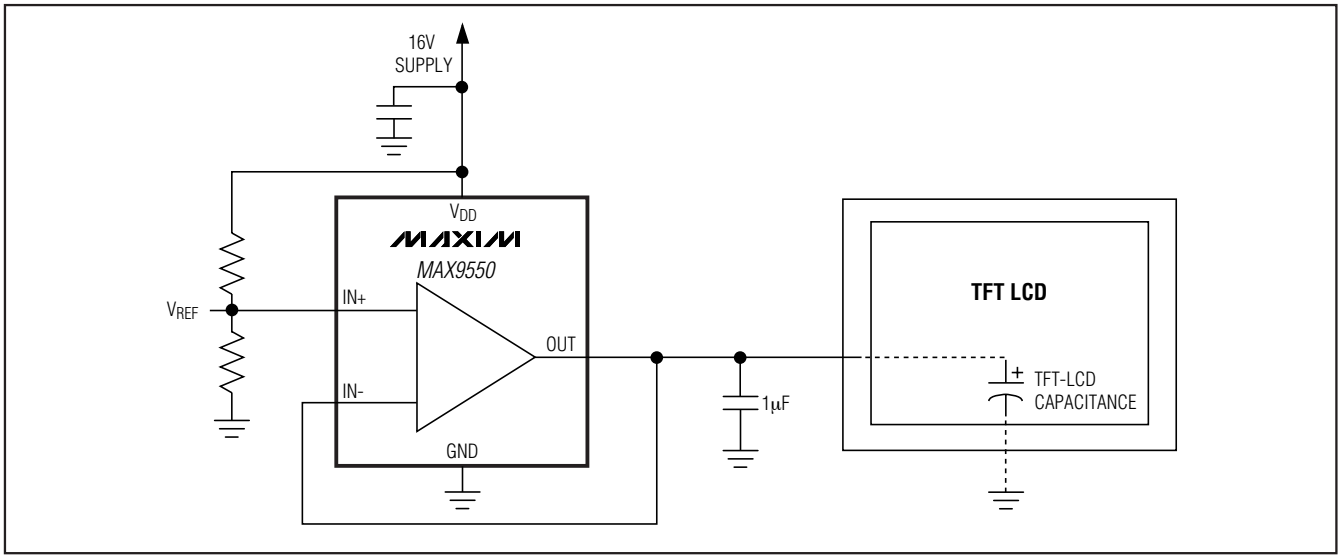
PART	AMPS	PIN-PACKAGE	PKG CODE	TOP MARK
MAX9550EZK+T	1	5 Thin SOT23-5	Z5-1	ADSG
MAX9550EUA+	1	8 µMAX-EP*	U8E-2	AABA
MAX9551EUA+	2	8 µMAX-EP*	U8E-2	—
MAX9552EUD+	4	14 TSSOP-EP*	U14E-3	—

Note: *All devices specified over the -40°C to +85°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed paddle.*

Typical Operating Circuit



µMAX is a registered trademark of Maxim Integrated Products, Inc.

High-Current VCOM Drive Buffers for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND) .....-0.3V to +22V
Any Other Pin to GND .....-0.3V to (V_{DD} + 0.3V)
IN+/IN- (current) .....±20mA
OUT, OUT_ (current).....1A
Continuous Power Dissipation (T_A = +70°C)
5-Pin Thin SOT23 (derate 2.7mW/°C above +70°C) ...219.1mW
8-Pin µMAX (derate 10.3mW/°C above +70°C) 824.7mW
14-Pin TSSOP (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 16V, GND = 0V, V_{CM} = V_{OUT} = V_{DD} / 2, C_L = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage Range	V_{DD}	Inferred from PSRR test and transient load test		7		20	V
Quiescent Current	I_{CC}	Per channel			2	4	mA
Low Output Voltage	V_{OL}	I_L = -4mA			0.04	0.1	V
High Output Voltage	V_{OH}	I_H = +4mA			V_{DD} - 0.04	V_{DD} - 0.1	V
Input Offset Voltage	V_{OS}			-10	+1	+10	mV
Input Bias Current	I_B				0.01	1	µA
Input Resistance	R_{IN}				1		MΩ
Common-Mode Input Voltage	CMVR	Inferred from CMRR		2		V_{DD} - 2	V
Common-Mode Rejection Ratio	CMRR	2V ≤ V_{IN} ≤ (V_{DD} - 2V)		80	96		dB
Power-Supply Rejection Ratio	PSRR	V_{OUT} = 3.5V, V_{DD} = 7V to 16V		80	96		dB
Continuous Output Current	I_O	V_{DD} = 7V, V_{OUT} = 3.5V, guaranteed by load, regulation test		55			mA
Output Load Regulation	LR1	I_{OUT} = 0mA to 50mA			6	13	mV
		I_{OUT} = 0mA to -50mA			6	13	
Output Load Regulation	LR2	V_{DD} = 7V, V_{OUT} = 3.5V	I_{OUT} = 0mA to -55mA		6.5	15	mV
			I_{OUT} = 0mA to 55mA		6.5	15	
Thermal Shutdown					+160		°C
Thermal Hysteresis					15		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 16V, GND = 0V, V_{CM} = V_{OUT} = V_{DD} / 2, C_L = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

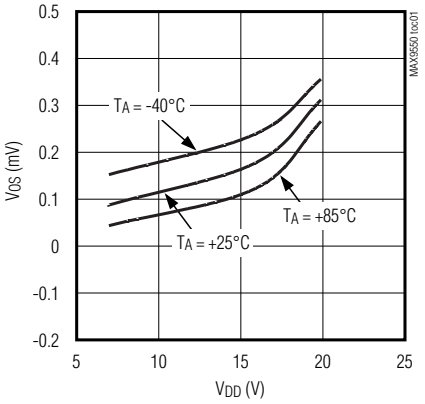
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS							
Settling Time	t_S	Settling to 0.1% of V_{OUT}, I_L = 0 to 600mA, C_L = 1µF, R_S = 2.2Ω, C_S = 0.1µF (Figure 1)			2.0		µs
Input Capacitance	C_{IN}				1.5		pF
Transconductance	gm	I_{OUT} = ±50mA			13		S
		I_{OUT} = ±500mA			42		
Transient Output Current	I_{OUTMAX}	A_V = 1	V_{DD} = 7V, V_{IN} = 1.5V pulse for 100µs	±200	±290		mA
			V_{DD} = 16V, V_{IN} = 1.5V pulse for 100µs	±600	±830		

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

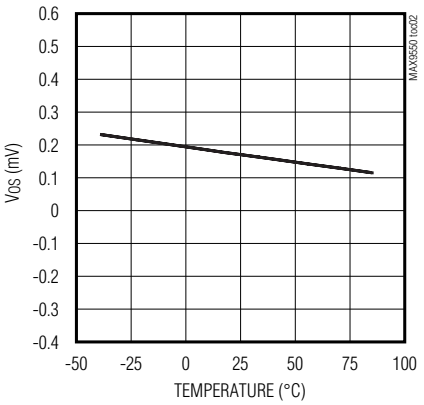
Typical Operating Characteristics

(V_{DD} = 16V, GND = 0V, V_{CM} = V_{OUT} = V_{DD} / 2, C_L = 1µF, T_A = +25°C, unless otherwise noted.)

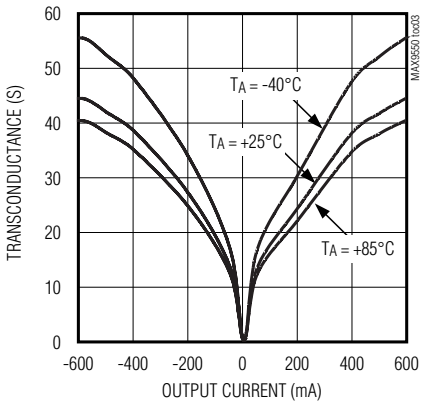
INPUT OFFSET VOLTAGE DEVIATION vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE



TRANSCONDUCTANCE vs. OUTPUT CURRENT

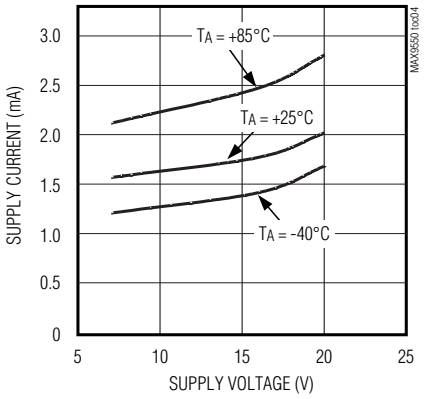


High-Current VCOM Drive Buffers for TFT LCDs

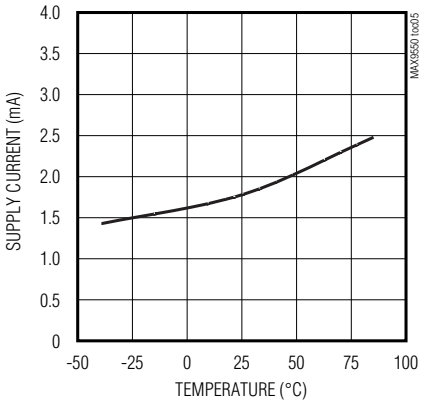
Typical Operating Characteristics (continued)

(V_{DD} = 16V, GND = 0V, V_{CM} = V_{OUT} = V_{DD} / 2, C_L = 1µF, T_A = +25°C, unless otherwise noted.)

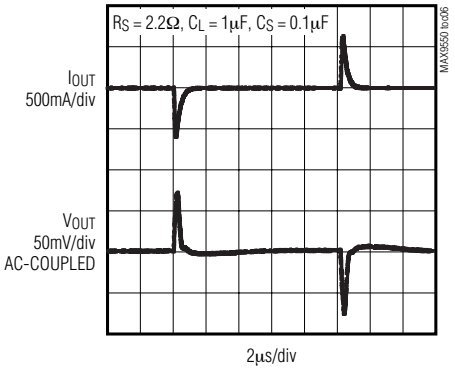
SUPPLY CURRENT vs. SUPPLY VOLTAGE



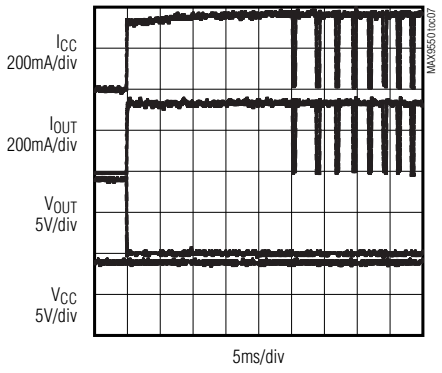
SUPPLY CURRENT vs. TEMPERATURE



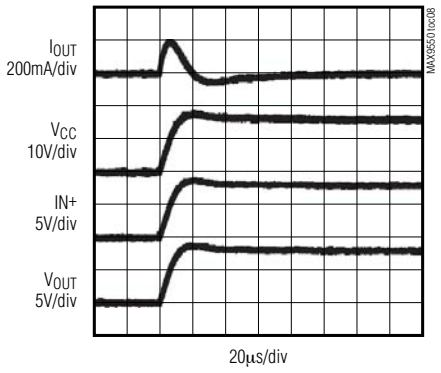
LOAD TRANSIENT (±600mA)



SHORT-CIRCUIT WAVEFORMS



STARTUP WAVEFORM



Pin Description

PIN				NAME	FUNCTION
MAX9550		MAX9551	MAX9552		
THIN SOT23	µMAX				
1	6	—	—	OUT	VCOM Output
2	4	4	11	GND	Ground
3	3	—	—	IN+	Positive Input
4	2	—	—	IN-	Negative Input
5	7	8	4	V_{DD}	Positive Supply Input
—	—	1	1	OUTA	VCOM Output A
—	—	3	3	INA+	Positive Input A
—	—	2	2	INA-	Negative Input A
—	1, 5, 8	—	—	N.C.	No Connection. Not internally connected.
—	—	5	5	INB+	Positive Input B
—	—	6	6	INB-	Negative Input B
—	—	7	7	OUTB	VCOM Output B
—	—	—	8	OUTC	VCOM Output C
—	—	—	9	INC-	Negative Input C
—	—	—	10	INC+	Positive Input C
—	—	—	12	IND+	Positive Input D
—	—	—	13	IND-	Negative Input D
—	—	—	14	OUTD	VCOM Output D
—	EP	EP	EP	EP	Exposed Paddle. EP is internally connected to GND. Connect EP to GND.

High-Current VCOM Drive Buffers for TFT LCDs

Detailed Description

The MAX9550/MAX9551/MAX9552 operational transconductance amplifiers (OTA) hold the VCOM voltage stable while providing the ability to source and sink a high current quickly (800mA typ) into a capacitive load such as the backplane of a TFT-LCD panel. The output settles to within 0.1% in less than 2µs. The fast settling time is achieved by increasing the transconductance of the buffer as the output current increases (see the *Typical Operating Characteristics*).

In addition, the MAX9550/MAX9551/MAX9552 directly drive the capacitive load in the VCOM layer of the TFT LCD without the need for a series resistor.

The MAX9550/MAX9551/MAX9552 unity-gain bandwidth is:

$$GBW = g_M / 2\pi C_{OUT}$$

where C_{OUT} is the capacitive load at the output and g_M is the transconductance.

To insure buffer stability, place a 1µF low-ESR capacitor as close to the OUT pin as possible. However, this value may be reduced if the TFT-LCD panel load provides some of the capacitance and the resistance in series when this capacitance is low. Connect the feedback at OUT using a Kelvin connection at the low-ESR capacitor.

Thermal Shutdown with Temperature Hysteresis

The MAX9550/MAX9551/MAX9552 are capable of high output currents and therefore, feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +160°C, the devices shut down. When the die cools down by 15°C, the devices turn on again.

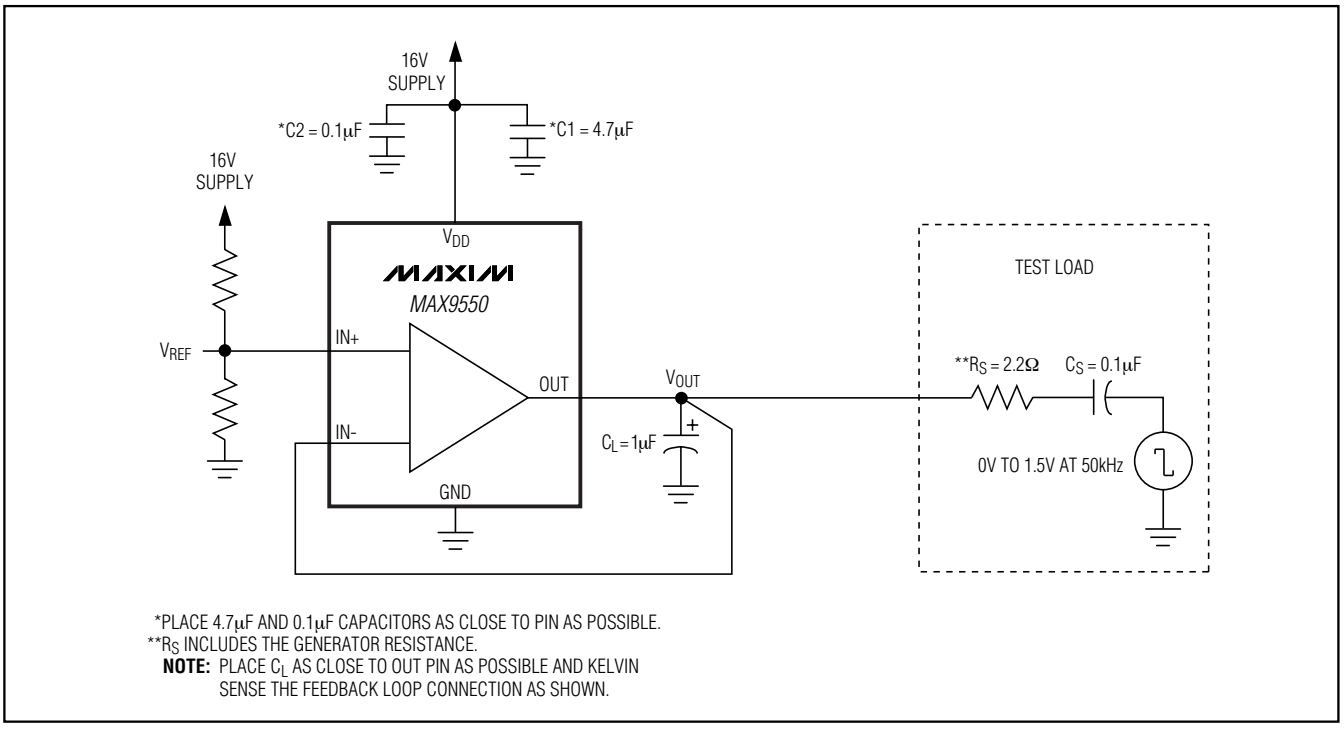


Figure 1. Settling Time Test Circuit

Applications Information

Output Load Capacitor

The output load capacitor must have a low ESR value (50mΩ or lower) and it must be placed as close as possible to the OUT pin to ensure buffer stability (see Figure 2). Ceramic capacitors are an excellent choice.

Power Supplies and Bypass Capacitors

The MAX9550/MAX9551/MAX9552 operate from a 6V to 20V single supply, or from ±3V to ±10V dual supplies. Proper supply bypassing ensures stability while driving high transient loads. The MAX9550/MAX9551/MAX9552 require minimum 4.7µF (C1) and 0.1µF (C2) power-supply bypass capacitors placed as close as possible to the power-supply pin (V_{DD}). See Figure 2. For dual-supply operation, use 4.7µF and 0.1µF bypass capacitors on both supplies (V_{DD} and GND) with each capacitor placed as close as possible to the V_{DD} and GND pins.

Layout and Grounding

The exposed paddle on the µMAX and TSSOP packages provides a low thermal resistance for heat dissipation. Solder the exposed paddle to a ground plane for best results. Do not route traces under these packages. For dual-supply operation, the exposed paddle (EP) must be electrically connected to the negative supply or it can be left unconnected.

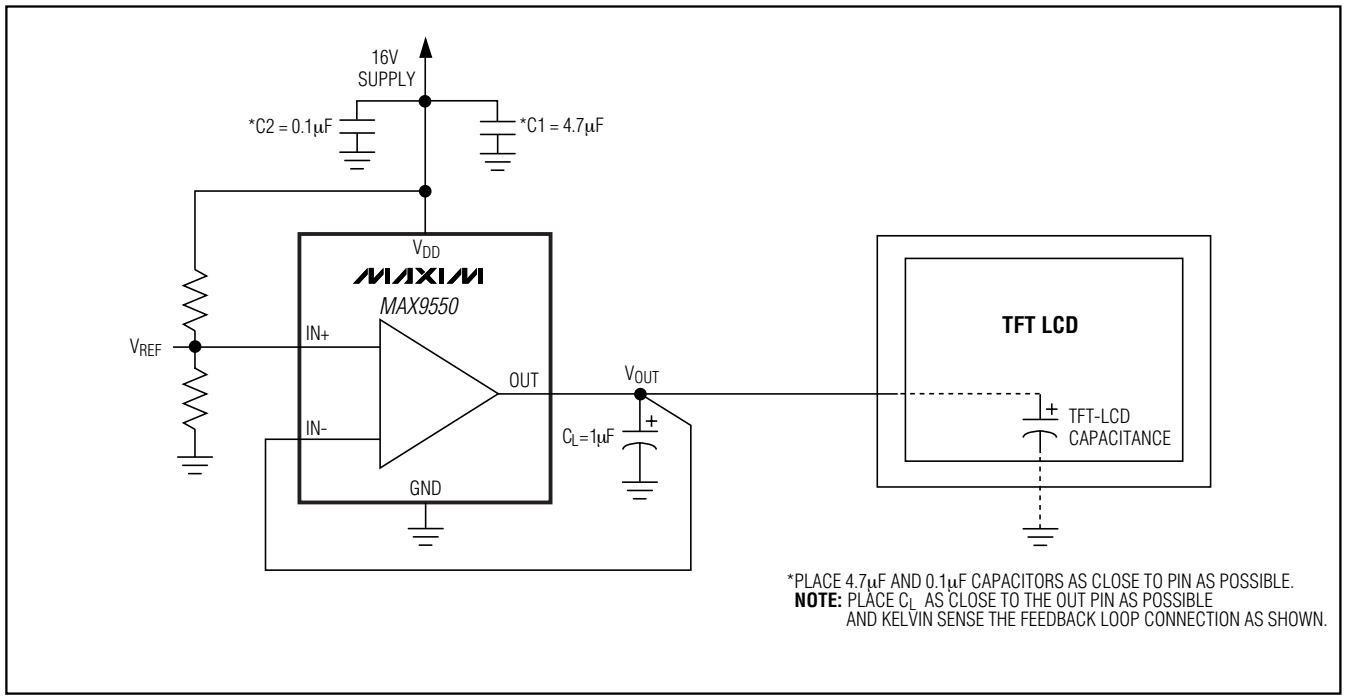
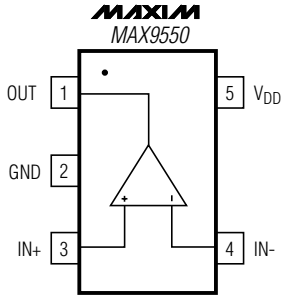


Figure 2. Typical TFT-LCD Backplane Drive Circuit

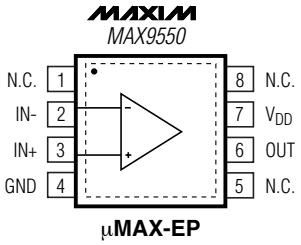
High-Current VCOM Drive Buffers for TFT LCDs

Pin Configurations

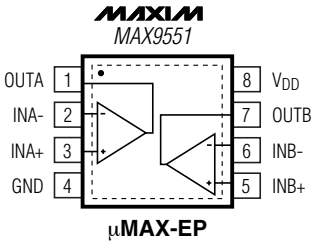
TOP VIEW



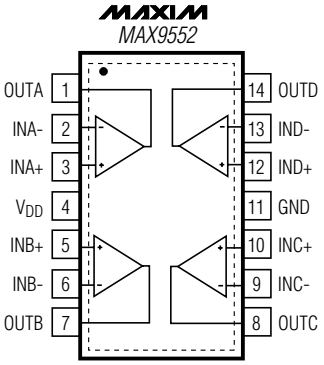
THIN SOT23



µMAX-EP



µMAX-EP



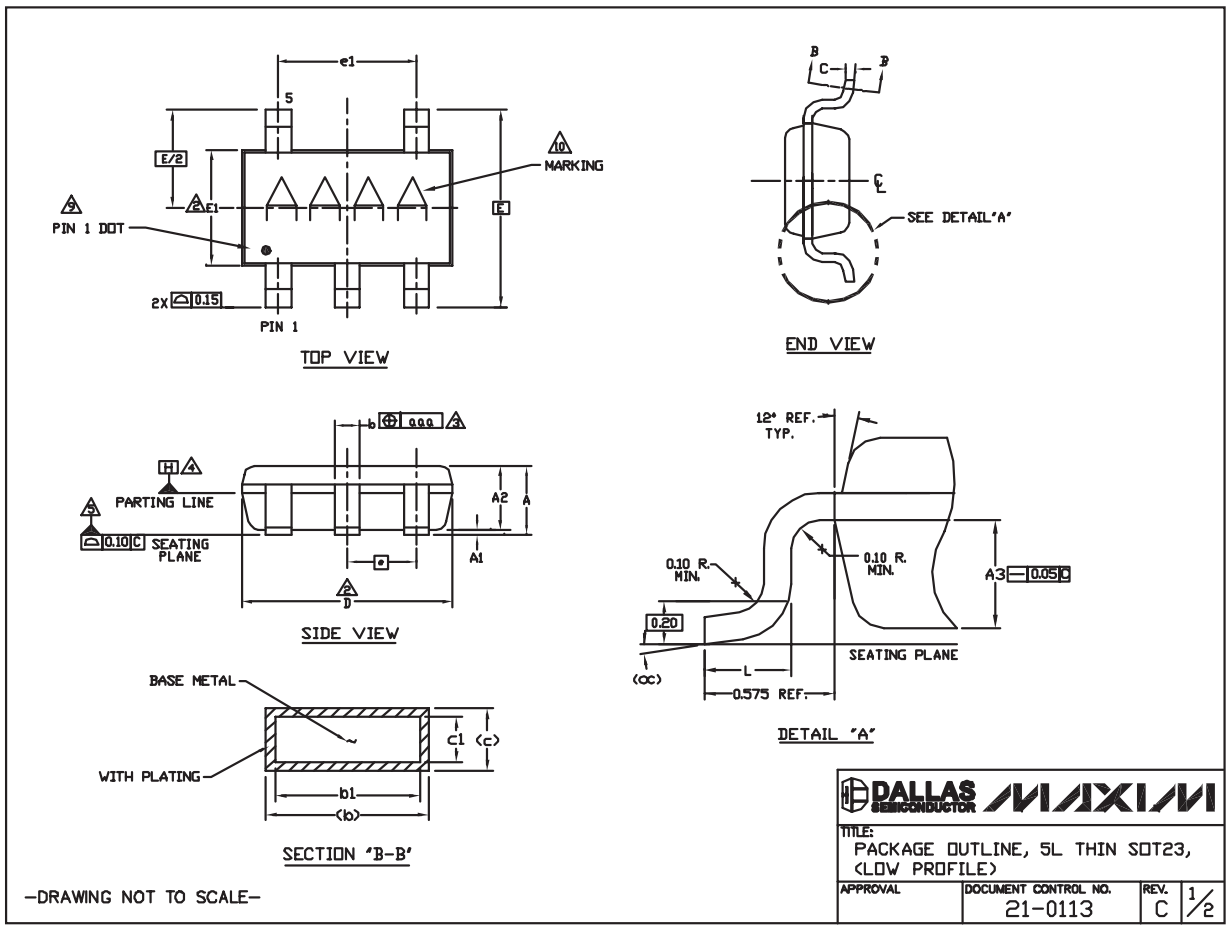
TSSOP-EP

Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



High-Current VCOM Drive Buffers for TFT LCDs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES, ONE PLANE IS THE SEATING PLANE, DATUM [-C-], AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
OC	0°	4°	8°
aaa		0.20	
Pkg. codes: Z5-1, Z5-2			

DALLAS SEMICONDUCTOR MAXIM

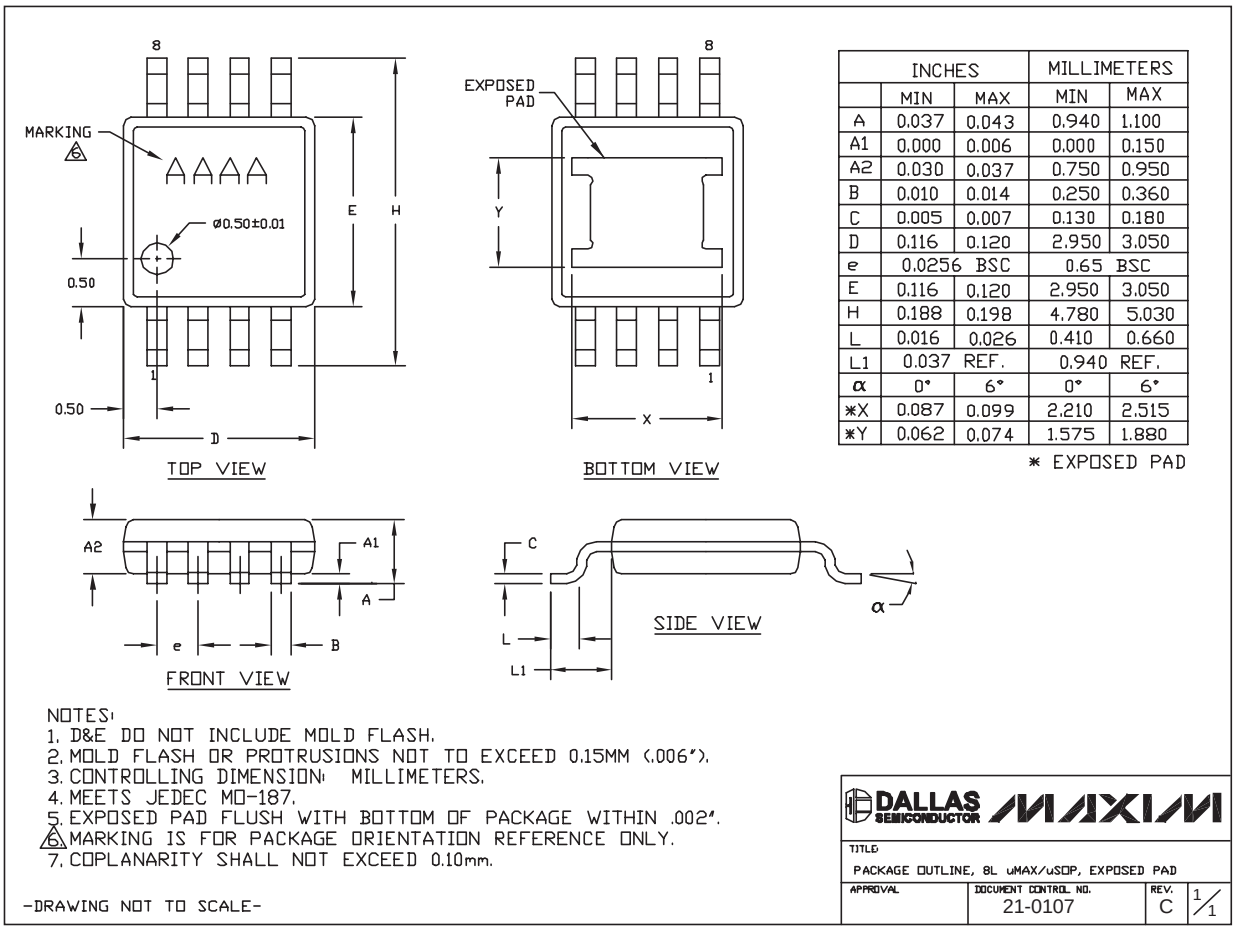
TITLE: PACKAGE OUTLINE, 5L THIN SOT23, (LOW PROFILE)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0113	C	2/2

-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037 REF.		0.940 REF.	
α	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515
*Y	0.062	0.074	1.575	1.880

* EXPOSED PAD

8L, µMAX, EXP PAD.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. COPLANARITY SHALL NOT EXCEED 0.10mm.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

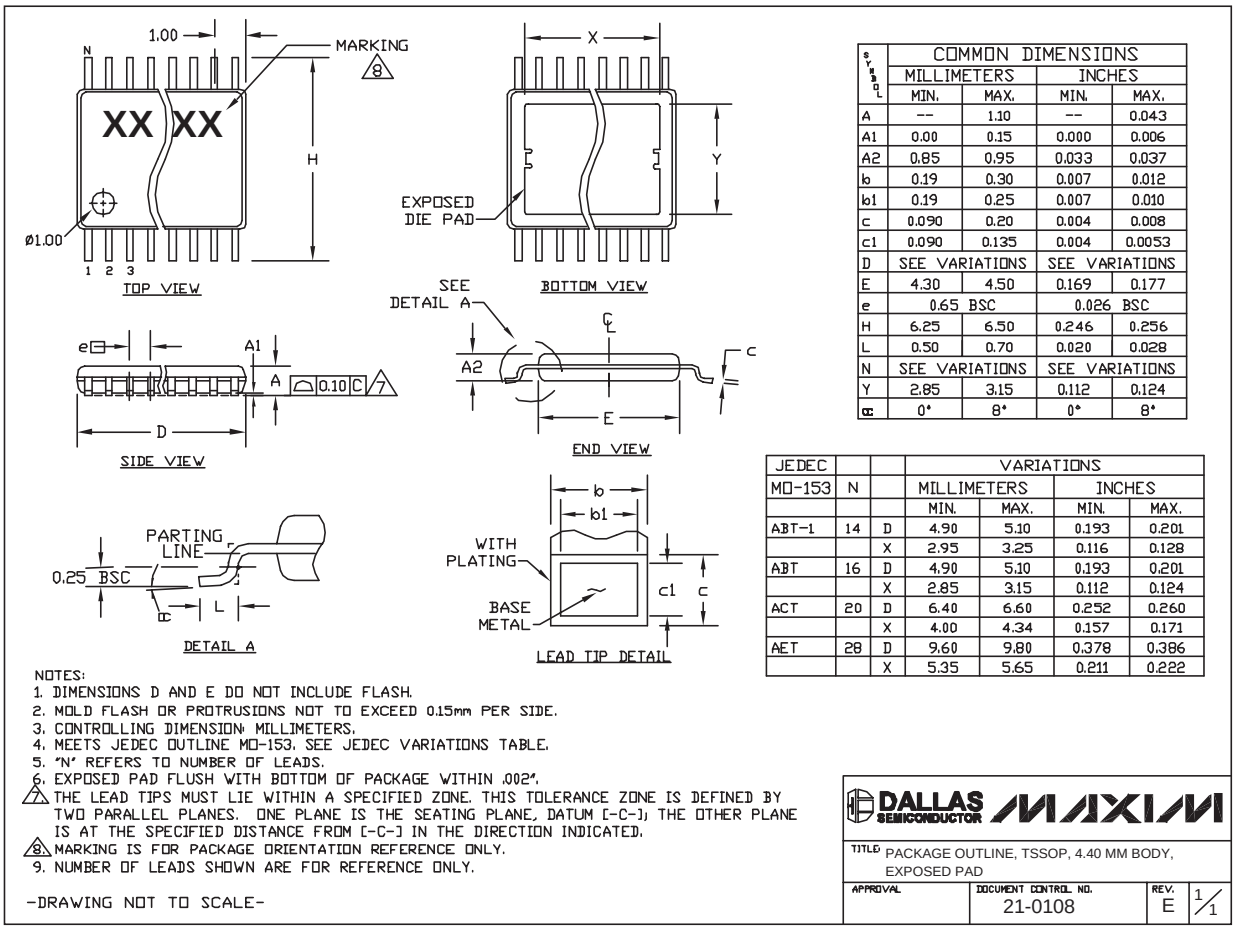
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0107	C	1/1

High-Current VCOM Drive Buffers for TFT LCDs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



TSSOP 4.4mm BODY.EPS

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	E	1/1

Revision History

Pages changed at Rev 3: 1, 2, 9, 10, 12